

CLAIMS

1. A digital circuit having a delay circuit for causing timing of a clock signal to be variable, characterized in that an amount of delay in the delay circuit is stabilized by using a delay synchronizing loop.
2. The digital circuit according to claim 1, characterized in that a driving current in the delay circuit is controlled to cause the amount of delay in the delay circuit to be variable.
3. The digital circuit according to claim 1, characterized in that the delay circuit has a delay amount setting voltage generating circuit for synthesizing two or more than two reference voltages.
4. The digital circuit according to claim 3, characterized in that the delay amount setting voltage generating circuit synthesizes reference voltages by means of a piece-wise linear approximation.
5. The digital circuit according to claim 3, characterized in that the delay amount setting voltage generating circuit is a voltage dividing type circuit.
6. The digital circuit according to claim 3, characterized in that the delay amount setting voltage generating circuit is a ladder type circuit.
7. The digital circuit according to claim 3, characterized in that the delay amount setting voltage generating circuit uses a MOSFET.
8. The digital circuit according to claim 2, characterized in that a circuit for controlling the driving current of the delay circuit is a current mirror type circuit.
9. The digital circuit according to claim 1, characterized in that the delay synchronizing loop has stabilizing means for stabilizing at a time of booting.